THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 28

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SADAYUKI KATO, HIROAKI ISHIHATA,
TAKESHI HORIE, SATOSHI INANO,
and TOSHIYUKI SHIMIZU

Appeal No. 96-0950
Application 07/727,932[1]

HEARD: APRIL 8, 1997

Before KRASS, BARRETT, and CARMICHAEL, *Administrative Patent Judges*.

CARMICHAEL, *Administrative Patent Judge*.

DECISION ON APPEAL

This is an appeal from the final rejection of Claims 1-7 and 9-14, which constitute all the claims remaining in the application.

We reverse.

[1] Application for patent filed July 10, 1991.

BACKGROUND

The claims

Appellants' Claim 1 is illustrative of the invention involved in the present appeal:

> 1. A data gathering system in a parallel computer, said data gathering system comprising:
>
> a common bus;
>
> a plurality of processors connected in parallel through said common bus,
>
> one of said plurality of processors being a reception processor which comprises a reception buffer for temporarily storing data gathered from other of said processors, and
>
> said other processors of said plurality of processors being transmitting processors, each respective transmitting processor comprising:
>
> a transmission buffer for temporarily storing the data to be transferred, and
>
> transfer control means for controlling data transmission from the transmission buffer to said common bus by checking a number of the data on said common bus, for sending a ready signal when ready to transfer the data and for determining an order of transfer by the respective transmitting processor of said plurality of transmitting processors; and
>
> AND means for receiving the ready signals from said plurality of processors and for outputting a reception signal to said plurality of processors.

The rejections

The Examiner's Answer lists the following prior art as relied upon in the rejection:

Quinquis	4,467,418	Aug. 21, 1984
Katzman et al. (Katzman)	4,228,496	Oct. 14, 1980

Claims 1-7 and 9-14 stand rejected under 35 U.S.C. § 103 as unpatentable over Quinquis and Katzman. Examiner's Answer at 3.

The invention

The claimed invention relates to a system for gathering and/or scattering data among a number of processors in a parallel processor computer. A gathering system collects data scattered among many processors into one processor. A scattering system distributes data from one processor to other processors. Specification at 1, lines 6-14.

As shown in Figure 6, the gathering system includes a bus L, a reception processor P0, an AND gate GA1, and transmitting processors P1, P2, and P3. Each transmitting processor P(n) includes a transmission buffer F(n) and a transfer control circuit U(n). Specification at 12, lines 23-36.

The transfer control circuit consults prestored values to determine an order of transfer for data in its own processor in relation to data in other processors. Different but coordinated

values are prestored in each transmitting processor's transfer control circuit as shown in Figure 14. The transfer control circuit checks the number of transfer data on the common bus L in accordance with a predetermined transfer schedule, and waits for an output from its own processor in accordance with the predetermined order. Specification at 10, line 7 through 11, line 4. The order of transfer is prestored in the gathering processor. Specification at 12, lines 1-9. In this way, the scattered data are gathered in the correct sequence and do not need to be rearranged by the gathering processor. Specification at 28, lines 9 through 34.

The prior art

Quinquis discloses a bus arbitration system in which each processor has its own allocator as shown in Figure 1. The allocator determines a priority code for itself, either at random or by presetting. Column 7, line 54 through Column 8, line 12. The system uses a data bus for transmitting data between two processors. When multiple processors desire to transmit data, they exchange control information over separate buses. The control information present on the separate buses at any given time reflects the priorities of the competing processors and whether the data bus is or is not occupied. Column 9, line 20

through column 10, line 27. For example, the occupation bus is in a 1 state during an exchange of data between a sending processor and a receiving processor and is in the 0 state when the data bus is at rest. Column 4, line 65 through column 5, line 2.

Katzman discloses in Figure 1 a centralized controller 37 for arbitrating requests for bus access among competing processors 33. The centralized controller 37 includes processor select logic 85 (Figure 3) which determines the priority of data transfers. Controller 37 has a separate select line 63 (Figure 2) to each processor. Controller 37 awards bus access to one processor by sending a signal over that processor's individual select line. Column 81, lines 16 through 68.

DISCUSSION

Claims 1-6 and 11-13

Claims 1-6 and 11-13 recite a data gathering system having transfer control means for (1) checking a number of data on a data bus and (2) determining an order of transfer by the respective transmitting processor of said plurality of transmitting processors.

The examiner states that Quinquis has means for performing function (1) and that it would have been obvious to incorporate

means for performing function (2) from Katzman. Appellants argue that Quinquis lacks means for performing either function and that the examiner has failed to indicate where the prior art suggests the desirability of adding the recited features to Quinquis as required under *In re Fritch*, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992). Reply Brief at 2. We agree with appellants.

1. Means For Checking a Number of Data On a Data Bus

According to the examiner, the recited means for checking is satisfied by Quinquis checking whether the occupation bus is a "1" or a "0." Examiner's Answer at 6. Appellants argue that Quinquis does not check a number of the data being transferred on the data bus. Appeal Brief at 7. We agree with appellants.

Even under the broadest reasonable interpretation of the recited means, we unable to say that checking whether the occupation bus is a "1" or a "0" constitutes checking a number of data on the data bus. Even if checking for a "1" or a "0" constituted checking a number of data on a bus, Quinquis checks for a "1" or a "0" on the occupation bus, not the data bus as required by the claims. Column 4, line 65 through column 5, line 2. Although the state of the occupation bus is intended to reflect whether or not the data bus is occupied, Quinquis does

not check a number of the data being transferred on the data bus. Furthermore, we do not find any suggestion in the cited art for adding to Quinquis a transfer control means for checking a number of data on the data bus as recited. Quinquis has no need to check a number of data on the data bus.

2. Means For Determining An Order of Transfer

Each processor is recited as having transfer control means for determining an order of transfer by the respective processor among a plurality. The examiner admits that Quinquis did not teach such means. Examiner's Answer at 3 and 6-7.

The examiner contends that it would have been obvious to incorporate Katzman's centralized transfer control means into each of Quinquis' processors because that would increase the throughput of the Quinquis system by allowing the individual processors to determine the order of transfer and thereby allow parallel determination. Examiner's Answer at 7.

The examiner cites nothing in the prior art to support the stated rationale. After carefully reviewing the cited art ourselves, we are unable to find any support or suggestion for the proposed combination. Katzman states that the bus controller is preferably separate and distinct from the processors 33. Column 17, lines 37-40. The bus controller and interprocessor

control of each processor coact in parallel with data processing in each processor so that there is no waste of processing power. Column 5, lines 13-22. Katzman's concern with wasting processing power does not encourage adding capacity in each processor for determining an order of transfer when the determination can be made centrally as disclosed.

When viewed as a whole, the cited prior art did not suggest a data gathering system having transfer control means for (1) checking a number of data on a data bus and (2) determining an order of transfer by the respective transmitting processor of said plurality of transmitting processors. Therefore, we do not sustain the rejection of Claims 1-6 and 11-13 under 35 U.S.C. § 103 as unpatentable over Quinquis and Katzman.

Claims 7 and 9

Claims 7 and 9 recite a data scattering system in which reception processors each comprise reception control means for selecting some of the data to be received from among all of the data broadcast by a transmitting processor. The selection is made in accordance with a predetermined reception count. Prior to any data transmission, an AND means receives ready signal from all of the reception processors and outputs a send signal back to

all of the reception processors. The send signal indicates that all of the reception processors are ready to receive data.

The examiner concedes that Quinquis did not disclose (1) the reception control means and (2) the AND means. The examiner contends that it would have been obvious to incorporate a reception control means from Katzman and AND means from well known practice in the art. Examiner's Answer at 4-5. Appellants argue that there was no suggestion to incorporate the recited means into Quinquis. Appeal Brief at 12 and 15. We agree with appellants.

1. Reception Control Means

The examiner states that it would have been obvious to incorporate Katzman's reception control means into the Quinquis system because that would allow Quinquis' system to select an amount of data to be received. Examiner's Answer at 5.

The examiner cites nothing in the prior art to support the stated rationale. After carefully reviewing the cited art ourselves, we are unable to find any support or suggestion for the proposed combination. No need was recognized in the art to allow each processor in Quinquis' system to select an amount of data to be received according to a predetermined reception count

out of data being broadcast by one transmitting processor. Nothing in the cited art suggests such a data scattering system.

2. AND Means

The examiner finds that use of AND means to determine when all processors are ready for a task (such as a data transmission) was well known in the art. Examiner's Answer at 7, lines 14-20.

The examiner's finding that it was well known in art to use AND means to determine when all processors are ready to transmit data does not lead one to the claimed invention. The recited AND means is for receiving ready signals from all the processors and for outputting a signal back to all the processors. As recited and as exemplified by Figure 6 of the Specification, AND means GA1 not only determines when all processors are ready to transmit data, it also outputs a signal to all the processors.

There is no apparent need to add the proposed AND means to Quinquis and/or Katzman because Quinquis and Katzman do not disclose data gathering or scattering between one processor and a plurality of other processors. Quinquis and Katzman are concerned with data exchanged between a single originating processor and a single terminating processor. Quinquis at Column 1, lines 18-27; Katzman at column 25, lines 23-25 and column 82, lines 1-5. Quinquis and Katzman had no need to determine whether

a plurality of processors are ready to receive and output a resultant signal to the plurality of transmitters. There is no need in the cited art to postpone transmission until multiple processors are ready to receive. There is no need in the cited art for each processor to receive a signal indicating that all processors are ready.

When viewed as a whole, the cited prior art did not suggest a data scattering system having (1) the recited reception control means and (2) the recited AND means. Therefore, we do not sustain the rejection of Claims 7 and 9 under 35 U.S.C. § 103 as unpatentable over Quinquis and Katzman.

Claims 10 and 14

Claims 10 and 14 recite a data gathering/scattering system that is switchable between a data gathering system and a data scattering system. The system includes (1) switching means in each processor to allow one processor to be switched into a data gatherer or scatterer and the other processors to be switched into transmitters or receivers and (2) AND means.

1. Switching Means

The examiner found that switching between data transmission and data reception was well known in the art and that Quinquis disclosed the individual processor being able to transmit and

receive data. Examiner's Answer at 8, lines 9-13. Further, the examiner held that it would have been obvious to add switching means into the Quinquis system because it would allow Quinquis to both transmit and receive data. Examiner's Answer at 5, lines 15-20.

The examiner's finding that switching between data transmission and data reception was well known in the art does not lead one to the claimed invention. The recited switching means does more than switch between data transmission and data reception. It switches a processor to form either a gathering system or a scattering system. As discussed above, neither Quinquis nor Katzman suggested a system for gathering or scattering data between a single processor and a plurality of processors. Therefore, there was no motivation to add to the cited art a switching means for switching a processor to form either a gathering system or a scattering system.

2. AND Means

The AND means of Claims 10 and 14 raise the same issues discussed above relating to the AND means.

When viewed as a whole, the cited prior art did not suggest a data gathering/scattering system having (1) the recited

switching means and (2) the recited AND means. Therefore, we do not sustain the rejection of Claims 10 and 14 under 35 U.S.C. § 103 as unpatentable over Quinquis and Katzman.

CONCLUSION

We have reversed the rejection of claims 1-7 and 9-14 under 35 U.S.C. § 103.

REVERSED

ERROL A. KRASS Administrative Patent Judge	)
LEE E. BARRETT Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
JAMES T. CARMICHAEL Administrative Patent Judge	)

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